Semiconductor varactor with reduced parasitic resistance

ABSTRACT OF THE INVENTION

A semiconductor varactor with reduced parasitic resistance. A contact isolation structure (32) is formed in a well region (20). The gate contact structures (70) are formed above the contact isolation structure (32) reducing the parasitic resistance. In addition, contact structures are formed on the gate layer (50) over the well regions (20) is a further embodiment to reduce the parasitic resistance.

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